What is claimed is:

1. A lead frame type of semiconductor apparatus comprising:

a die pad on which a semiconductor chip is mounted;

ground terminals which are to be grounded;

power supply terminals which are connected to a power supply;

inner leads connected to the ground terminals and power supply terminals, in which a pair of adjacent inner leads for power supply terminal and ground terminal are extended inwardly;

a chip capacitor mounting pad which is provided at inner ends of the extended inner leads; and

a chip capacitor which is mounted on the chip capacitor mounting pad so that a decoupling capacitor is provided.

2. A semiconductor apparatus according to claim 1, wherein

the chip capacitor mounting pad is adhered to the extended inner leads with a conductive adhesive.

3. A semiconductor apparatus according to claim 1, wherein

a plurality of pairs of inner leads are extended inwardly so that a plurality of chip capacitor mounting pads and a plurality of chip capacitors are provided as well; and

the number of chip capacitors or total amount of capacity of the chip capacitors becomes equivalent for every side of the die pad.

4. A lead frame type of semiconductor apparatus comprising:

a die pad on which a semiconductor chip is mounted;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power, in which each one of the ground terminals and each one of the power supply terminals are arranged to be adjacent each other so that a plurality of pairs of ground/power supply terminals are formed;

inner leads connected to the ground terminals and power supply terminals;

high dielectric constant material provided between each pair of the ground/power supply terminals so that a decoupling capacitor is formed therein.

5. A semiconductor apparatus according to claim 4, wherein

the high dielectric constant material is ceramics, such as alumina (aluminum oxide) and titan oxide.

6. A semiconductor apparatus according to claim 4, wherein

the high dielectric constant material is formed by a sintering treatment in the fabrication process of a lead frame.

7. A lead frame type of semiconductor apparatus comprising:

a die pad which comprises a chip mounting area on which a

semiconductor chip is mounted and a ground bonding area, which is extended outwardly from the chip mounting area;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals; and

chip capacitors connected between the ground bonding area and inner leads connected to the power supply terminals to form decoupling capacitors.

8. A semiconductor apparatus according to claim 7, wherein

the semiconductor chip is provided at an surface with surface electrodes for power supply and ground,

the ground bonding area is connected to the surface electrodes for ground of the semiconductor chip with bonding wires, while the inner leads connected to the power supply terminals are connected to the surface electrodes for power supply of the semiconductor chip with bonding wires.

9. A semiconductor apparatus according to claim 7, wherein

the die pad is provided with a groove to define the chip mounting area and ground bonding area.

10. A lead frame type of semiconductor apparatus comprising:

a die pad on which a semiconductor chip is mounted, in which the die pad is divided into even number of areas to form first and second areas;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals, in which the inner leads connected to the ground terminals are connected to the first area of the die pad and the inner leads connected to the power supply terminals are connected to the second area of the die pad;

chip capacitors connected between the first area and second area of the die pad to form decoupling capacitors.

11. A semiconductor apparatus according to claim 10, wherein the die pad is divided into two areas.

12. A semiconductor apparatus according to claim 10, wherein the die pad is divided into four areas, in which the first and second areas are arranged in turn.

13. A lead frame type of semiconductor apparatus comprising:

a die pad which comprises a chip mounting area on which a

semiconductor chip is mounted and ground bonding areas, which are formed by extending outwardly the opposite two sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals;

power supply bonding areas which are arranged between the die pad and inner lead and are connected to the inner leads connected to the power supply terminals, wherein the power supply bonding areas are arranged at the opposite two sides of the die pad; and

chip capacitors connected between the die pad and the power supply bonding areas to form decoupling capacitors.

14. A semiconductor apparatus according to claim 13, wherein

the die pad is provided with a groove to define the chip mounting area and ground bonding areas.

15. A lead frame type of semiconductor apparatus comprising:

a die pad which comprises a chip mounting area on which a semiconductor chip is mounted and a ground bonding area, which are formed by extending outwardly all the sides of the die pad so that the ground bonding area surround the chip mounting area;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals;

power supply bonding areas which are arranged between the ground bonding area of the die pad and inner lead and are connected to the inner leads connected to the power supply terminals; and

chip capacitors connected between the ground bonding area and the power supply bonding areas to form decoupling capacitors.

16. A semiconductor apparatus according to claim 15, wherein

the die pad is provided with a groove surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

17. A semiconductor apparatus according to claim 16, wherein

the number of chip capacitors or total amount of capacity of the chip capacitors becomes equivalent for every side of the die pad.

18. A lead frame type of semiconductor apparatus comprising:

a die pad which comprises a chip mounting area on which a semiconductor chip is mounted and a ground bonding area, which are formed by extending outwardly all the sides of the die pad so that the ground bonding area surround the chip mounting area;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals;

power supply bonding areas which are arranged between the ground bonding area of the die pad and inner lead and are connected to the inner leads connected to the power supply terminals; and

a high dielectric constant material arranged between the ground bonding area and the power supply bonding areas to form decoupling capacitors.

19. A semiconductor apparatus according to claim 18, wherein

the die pad is provided with a groove surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

20. A semiconductor apparatus according to claim 18, wherein

the high dielectric constant material is ceramics, such as alumina (aluminum oxide) and titan oxide.

21. A lead frame type of semiconductor apparatus comprising:

a die pad which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

inner leads connected to the ground terminals and power supply terminals, in which the inner leads connected to the power supply terminals are connected to the power supply bonding area of the die pad; and

a high dielectric constant layer formed on the die pad;

a metal layer formed between the high dielectric constant layer and die pad to have a chip mounting area on which a semiconductor chip is mounted and a ground bonding area surrounding the chip mounting area.

22. A semiconductor apparatus according to claim 21, wherein

the metal layer is provided with a groove surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

23. A semiconductor apparatus according to claim 21, wherein

the high dielectric constant layer is of ceramics, such as alumina (aluminum oxide) and titan oxide.

24. A semiconductor apparatus comprising:

an organic material substrate;

a die pad formed on the organic material substrate, a semiconductor chip being mounted on the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals, in which adjacent two of the first and second conducive patterns are extended inwardly;

chip capacitor mounting pads which are provided at inner ends of the extended first and second conductive patterns; and

chip capacitors which are mounted on the chip capacitor mounting pads so that a decoupling capacitor is provided.

25. A semiconductor apparatus according to claim 24, wherein

the chip capacitor mounting pad are adhered to the first and second conductive patterns with a conductive adhesive.

26. A semiconductor apparatus according to claim 24, wherein

the number of chip capacitors or total amount of capacity of the chip capacitors becomes equivalent for every side of the die pad.

27. A semiconductor apparatus according to claim 24, wherein the organic material substrate is provided with cavities in which the chip capacitors are mounted therein.

28. A semiconductor apparatus according to claim 27, wherein the chip capacitor mounting pads are arranged at bottoms of the cavities, each of which is provided with side wall plating electrically connected to the corresponding first and second conductive patterns.

29. A semiconductor apparatus comprising:

an organic material substrate;

a die pad formed on the organic material substrate to have a chip mounting area on which a semiconductor chip is mounted and a ground bonding area which is formed by extending outwardly each side of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals; and

chip capacitors which are arranged between the second conductive patterns and the ground bonding area so that a decoupling capacitor is provided.

30. A semiconductor apparatus according to claim 29, wherein

the semiconductor chip is provided at an surface with surface electrodes for power supply and ground,

the ground bonding area is connected to the surface electrodes for ground of the semiconductor chip with bonding wires, while the second conductive patterns are connected to the surface electrodes for power supply of the semiconductor chip with bonding wires.

31. A semiconductor apparatus according to claim 29, wherein

the die pad is provided with a projection or ridge to define the chip mounting area and ground bonding area.

32. A semiconductor apparatus according to claim 29, wherein

the organic material substrate is provided with cavities in which the chip capacitors are mounted therein.

33. A semiconductor apparatus according to claim 32, wherein

the chip capacitor mounting pads are arranged at bottoms of the cavities, each of which is provided with side wall plating electrically connected to the corresponding first and second conductive

patterns.

34. A semiconductor apparatus comprising:

an organic material substrate;

a die pad formed on the organic material substrate on which a semiconductor chip is mounted, in which the die pad is divided into even number of areas to form first and second areas;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals and the first area of the die pad;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals and the second area of the die pad; and

chip capacitors which are arranged between the first and second areas of the die pad so that a decoupling capacitor is provided.

35. A semiconductor apparatus according to claim 34, wherein the die pad is divided into two areas.

36. A semiconductor apparatus according to claim 34, wherein the die pad is divided into four areas, in which the first and

second areas are arranged in turn.

37. A semiconductor apparatus comprising:

an organic material substrate;

a die pad which is formed on the organic material substrate and comprises a chip mounting area on which a semiconductor chip is mounted and ground bonding areas, which are formed by extending outwardly the opposite two sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals;

power supply bonding areas which are arranged between the die pad and the first and second conductive patterns and are connected to the first conductive patterns, wherein the power supply bonding areas are arranged at the opposite two sides of the die pad; and

chip capacitors which are arranged between the die pad and power supply boding area so that a decoupling capacitor is provided.

38. A semiconductor apparatus according to claim 37, wherein

the die pad is provided with a projection or ridge to define the chip mounting area and ground bonding areas.

39. A semiconductor apparatus according to claim 37, wherein the organic material substrate is provided with cavities in which the chip capacitors are mounted therein.

40. A semiconductor apparatus comprising:

an organic material substrate;

a die pad which is formed on the organic material substrate and comprises a chip mounting area on which a semiconductor chip is mounted and ground bonding areas, which are formed by extending outwardly to surround the chip mounting area;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals;

power supply bonding areas which are arranged between the ground bonding area of the die pad and the first and second conductive patterns, the power supply bonding area being connected to the second conductive patterns; and

chip capacitors which are arranged between the ground bonding area and power supply bonding area so that a decoupling capacitor is provided.

41. A semiconductor apparatus according to claim 40, wherein the die pad is provided with a projection or ridge surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

42. A semiconductor apparatus according to claim 40, wherein the number of chip capacitors or total amount of capacity of the chip capacitors becomes equivalent for every side of the die pad.

43. A semiconductor apparatus comprising:

an organic material substrate;

a die pad which is formed on the organic material substrate and comprises a chip mounting area on which a semiconductor chip is mounted and ground bonding areas, which are formed by extending outwardly to surround the chip mounting area;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals;

power supply bonding areas which are arranged between the ground bonding area of the die pad and the first and second conductive patterns, the power supply bonding area being connected to the second conductive patterns; and

a high dielectric constant material arranged between the ground bonding area and the power supply bonding areas to form decoupling capacitors.

44. A semiconductor apparatus according to claim 43, wherein

the die pad is provided with a projection or ridge surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

45. A semiconductor apparatus according to claim 43, wherein

the high dielectric constant material is ceramics, such as alumina (aluminum oxide) and titan oxide.

46. A semiconductor apparatus comprising:

an organic material substrate;

a die pad which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the organic material substrate and are connected to the ground terminals;

second conductive patterns which are formed on the organic material substrate and are connected to the power supply terminals;

a high dielectric constant layer formed on the die pad; and

a metal layer formed between the high dielectric constant layer and die pad to have a chip mounting area on which a semiconductor chip is mounted and a ground bonding area surrounding the chip mounting area.

47. A semiconductor apparatus according to claim 46, wherein

the metal layer is provided with a projection or ridge surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

48. A semiconductor apparatus according to claim 46, wherein

the high dielectric constant layer is of ceramics, such as alumina (aluminum oxide) and titan oxide.

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